REMARKS/ARGUMENTS

Claims 1-19 are pending in the application. Claims 3, 9, and 16 have been cancelled.

Claims 1, 4, 7, 10, 14, and 17 have been amended.

Claims 1, 5, 7, 14, and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by

Swoboda et al., U.S. Patent No. 6,643,803 (hereinafter "Swoboda"). Claims 2, 8, and 15 were

rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Sato, U.S.

Patent No. 5,903,768 (hereinafter "Sato"). Claims 3-4, 6, 9-11, 16-17, and 19 were rejected

under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam et al., U.S.

Patent No. 6,285,974 (hereinafter "Mandyam"). Claims 12-13 were rejected under 35 U.S.C.

§103(a) as being unpatentable over Swoboda in view of Mandyam in further view of Hennessy

and Patterson, Computer Organization and Design, 2nd Edition, 1998 (hereinafter "Hennessy").

Claim Rejections Under 35 U.S.C. §102(e)

Claims 1, 5, 7, 14, and 18 were rejected under 35 U.S.C. §102(e) as being anticipated by

Swoboda. Swoboda generally discloses emulation and debug circuitry that can be incorporated

into a variety of digital systems (*See* Abstract).

Swoboda does not disclose generating with a No-operation (NOP) pseudo-random

generator a neutral instruction that causes an architectural state value for said processor to be

ascertained, as recited by claims 1, 7, and 14 as amended. The Office Action cites Claim 4 of

Swoboda, which states:

> jamming circuitry connected to the instruction pipeline operable to jam an access for a
> system resource in response to an access command received by the test port circuitry into
> the bubble detected by the detection circuitry, whereby the access of the system resources

in response to the access command is performed without delaying the instruction pipeline when the processor is not in the debug suspend state.
(*See* Swoboda, Claim 1).

No mention is made of a NOP pseudo-random generator in Swoboda. Therefore, Swoboda does not disclose generating with a NOP pseudo-random generator a neutral instruction that causes an architectural state value for said processor to be ascertained. Applicants respectfully submit, therefore, that elements of claim 1, 7, and 14 are neither shown nor suggested by the cited reference. Claims 5 and 18 depend from claims 1 and 14, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 1, 5, 7, 14, and 18 under 35 U.S.C. §102(e) is respectfully requested.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 2, 8, and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Sato. Sato discloses a pipelined microprocessor capable of avoiding pipeline stalls (*See* Abstract). One of the disclosed methods is by inserting a NOP operation into the pipeline (*See* Sato, Col. 2, Lines 4-14).

Neither Swoboda, Sato, nor any combination thereof discloses generating with a NOP pseudo-random generator a neutral instruction that causes an architectural state value for said processor to be ascertained, as recited by claims 1, 7, and 14.

Applicants respectfully submit, therefore, that elements of claims 1, 7, and 14 are neither shown nor suggested by the cited references. Claims 2, 8, and 15 depend from claims 1, 7, and 14, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 2, 8, and 15 under 35 U.S.C. §103(a) is respectfully requested.

Claims 3-4, 6, 9-11, 16-17, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam. Mandyam discloses detecting architectural violations in a multiprocessor computer system using a random test generator.

Neither Swoboda, Mandyam, nor any combination thereof discloses generating with a NOP pseudo-random generator a neutral instruction that causes an architectural state value for said processor to be ascertained, as recited by claims 1, 7, and 14. The random test generator of Mandyam generates test instructions, but not no-operation instructions.

Applicants respectfully submit, therefore, that elements of claims 1, 7, and 14 are neither shown nor suggested by the cited references. Claims 3-4, 6, 9-11, 16-17, and 19 depend from claims 1, 7, and 14, respectively. Accordingly reconsideration and withdrawal of the rejection of claims 3-4, 6, 9-11, 16-17, and 19 under 35 U.S.C. §103(a) is respectfully requested.

Claims 12-13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Swoboda in view of Mandyam in further view of Hennessy. Hennessy is a computer textbook that discloses AND and OR operations.

Neither Swoboda, Mandyam, Hennessy, nor any combination thereof discloses generating with a NOP pseudo-random generator a neutral instruction that causes an architectural state value for said processor to be ascertained, as recited by claim 7.

Applicants respectfully submit, therefore, that elements of claim 7 are neither shown nor suggested by the cited references. Claims 12-13 depend from claim 7. Accordingly reconsideration and withdrawal of the rejection of claims 12-13 under 35 U.S.C. §103(a) is respectfully requested.

Application No.: 09/751,761
Amendment dated: April 13, 2005
Reply to Office Action dated: January 13, 2005

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600.**

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON

Dated: April 13 ,2005   By: _Stephen T. Neal_
                 Stephen T. Neal
                 (Reg. No. 47,815)
                 Attorneys for Intel Corporation

KENYON & KENYON
333 West San Carlos St., Suite 600
San Jose, CA 95110

Telephone: (408) 975-7500
Facsimile: (408) 975-7501